

AMENDMENT

In the Claims:

1. (original) A circuit for reading a memory cell, the circuit comprising:
a read node operable to receive a read current from the memory cell;
a first current source operable to provide a first bias current to the read node;
a first transistor having a control terminal and a first conduction terminal coupled to the read node;
a reference node;
a reference generator operable to provide a reference current to the reference node;
a second current source operable to provide a second bias current to the reference node; and
a second transistor having a control terminal coupled to the read node and having a first conduction terminal coupled to the reference node.

2. (original) The circuit of claim 1, further comprising:
first and second supply nodes;
wherein the first and second current sources are coupled to the first supply node;
and
wherein the first and second transistors each have a respective second conduction terminal coupled to the second supply node.

3. (original) The circuit of claim 1 wherein the first bias current equals the second bias current.

4. (original) The circuit of claim 1 wherein:
the first and second current sources each comprise a respective PMOS transistor;
and
the first and second transistors each comprise a respective NMOS transistor.

5. (original) The circuit of claim 1, further comprising:
a third transistor having a control terminal and a conduction terminal coupled to the read node; and
a fourth transistor having a control terminal and a conduction terminal coupled to the reference node.

6. (original) The circuit of claim 1, further comprising:
a bias generator operable to generate a bias voltage; and
wherein the first and second current sources are operable to generate the first and second bias currents in response to the bias voltage.

7. (original) The circuit of claim 1, further comprising a comparator having first and second input terminals respectively coupled to the read and reference nodes.

8. (original) The circuit of claim 1, further comprising a precharger coupled to the read node.

9. (original) A method for reading a memory cell, the method comprising:
sourcing a first bias current to a read node;
sinking a read current from the read node;
sinking from the read node a first difference current that is inversely proportional to the read current;
sourcing a second bias current to a reference node;
sinking a reference current from the read node; and
sinking from the reference node a second difference current that is inversely proportional to the read current.

10. (original) The method of claim 9 wherein the first bias current equals the second bias current.

11. (original) The method of claim 9, further comprising comparing a voltage on the read node to a voltage on the reference node to determine a data value stored in the memory cell.

12. (original) The method of claim 9, further comprising sinking from the read node a third difference current that is inversely proportional to the read current.

13. (original) The method of claim 9, further comprising sinking from the reference node a third difference current that is proportional to the read current.

14. - 28. Cancelled.